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EXAMINER	
BRADLEY, MATTHEW A	

ART UNIT	PAPER NUMBER
2187	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/723,009	RAMAKRISHNAN, SIVA	
	Examiner	Art Unit	
	Matthew Bradley	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-23 and 25-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3-23, and 25-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 29 October 2007 has been entered.

Claim Status

Claims 1, 3-23, and 25-29 remain pending and are ready for examination.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims **1**, **3-4**, **9**, and **18-21** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hovis et al (U.S. 5,812,817), hereinafter referred to as Hovis, in view of Harris (U.S. 6,601,151), hereinafter referred to as Harris.

As per independent claim **1**, Hovis teach,

- a compression cache to store a plurality of uncompressed data, wherein the compression cache is organized as a sectored cache that has associated tags that are on-die; (Figure 1 as taught in Column 2 lines 35-

37 and the sectored cache being taught by Hovis as segments of memory within the uncompressed storage cache in Column 2 lines 50-51)

- wherein a tag match is performed between a memory access request and the associated tags and a hit signal is sent to a memory controller coupled to the main memory to schedule an uncompressed data access from the compression cache if a hit occurs (Column 2 lines 44-59)
- a compressed memory to store a plurality of compressed data; and (Figure 1 as taught in Column 2 lines 37-38)
- a compressed memory pointer table (CMPT) to store a plurality of pointers (Column 1 lines 44-51)

Hovis does not explicitly teach, the apparatus to assign a higher priority to compressed memory read operations in comparison to other operations.

Harris teaches, the apparatus to assign a higher priority to compressed memory read operations in comparison to other operations (Figure 4 as taught in Column 7 line 58 to Column 8 line 24).

Hovis and Harris are analogous art because they are from the same field of endeavor namely, memory systems.

At the time of invention, it would have been obvious to one of ordinary skill in the art, having both the teachings of Hovis and Harris before him/her to combine the memory read prioritization of Harris with Hovis for the benefit of enhanced and improved performance.

The suggestion for doing so would have been that, processor performance can be enhanced by ascribing memory read requests higher priority than other requests (Column 7 line 58 to Column 8 line 24). Further, as further taught in the aforementioned citing of Harris, write requests are given the lowest priority. Thus, Harris obviates that which is instantly claimed in that the system assigns a higher priority to read operations in comparison to other operations.

Therefore, it would have been obvious to combine Hovis with Harris for the memory read prioritization to obtain the invention as specified in claims 1, 3-4, 9, and 18-21.

As per dependent claim **3**, the combination of Hovis and Harris teach, wherein the compression cache has a plurality of associated tags that are incorporated within a memory interface coupled to the apparatus (Column 3 lines 3-15 of Hovis).

As per dependent claim **4**, the combination of Hovis and Harris teach, wherein the plurality of pointers are to the plurality of compressed data based on a plurality of cache block addresses (Column 3 lines 3-8 of Hovis).

As per dependent claim **9**, the combination of Hovis and Harris teach, wherein the CMPT is to store the plurality of pointers to the plurality of compressed data sequentially based on memory addresses for the plurality of compressed data (Figure 3 as taught in Column 3 lines 25-39 of Hovis).

As per independent claim **18**, the combination of Hovis and Harris teach,

- a processor; and (Figure 4 item 22 of Hovis)

- a main memory, coupled to the processor, with a (Figure 4 item 10 of Hovis)
- a compression cache to store a plurality of uncompressed data; wherein the compression cache is organized as a sectored cache that has associated tags that are on-die, (Figure 1 as taught in Column 2 lines 35-37 and the sectored cache being taught by Hovis as segments of memory within the uncompressed storage cache in Column 2 lines 50-51)
- wherein a tag match is performed between a memory access request and the associated tags and a hit signal is sent to a memory controller coupled to the main memory to schedule an uncompressed data access from the compression cache if a hit occurs; (Column 2 lines 44-59 of Hovis)
- a compressed memory to store a plurality of compressed data; and (Figure 1 as taught in Column 2 lines 37-38 of Hovis)
- a compressed memory pointer table (CMPT) to store a plurality of pointers (Column 1 lines 44-51 of Hovis)
- and to assign a higher priority to compressed memory read operations in comparison to other operations (Figure 4 as taught in Column 7 line 58 to Column 8 line 24 of Harris).

As per dependent claim **19**, the combination of Hovis and Harris teach, wherein the compression cache is a sectored cache (the sectored cache being taught by Hovis as segments of memory within the uncompressed storage cache in Column 2 lines 50-51).

As per dependent claim **20**, the combination of Hovis and Harris teach, wherein the compression cache has a plurality of associated tags that are incorporated within a memory interface (Column 3 lines 3-15 of Hovis).

As per dependent claim **21**, the combination of Hovis and Harris teach, wherein the plurality of pointers are to the plurality of compressed data based on a plurality of cache block addresses (Column 3 lines 3-8 of Hovis).

Claims **14**, **16-17**, **22-23**, and **25-29** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hovis in view of Van Doren et al (U.S. 6,202,126) hereinafter referred to as Van Doren.

As per independent claim **14**, Hovis teach,

- receiving a memory address for the memory operation; (Column 3 lines 54-57 of Hovis taught as the access to the memory requiring a memory address for such access to occur)
- storing a plurality of compressed data in a compressed memory in a main memory; and (Figure 1 as taught in Column 2 lines 37-38 of Hovis)
- performing a tag match between the memory address and a first cache of a memory interface coupled to the main memory storing a plurality of tags for a compression cache in the main memory (Column 2 lines 44-59 of Hovis)
- accessing a plurality of uncompressed data from the compression cache responsive to an uncompressed access scheduling by a memory

controller if the tag match resulted in a hit, and (Column 3 lines 54-57 of Hovis)

Hovis does not teach a victim buffer.

Van Doren teach,

- if the tag match resulted in a miss, accessing the plurality of uncompressed data directly from a victim buffer of the memory interface if the plurality of uncompressed data is present in the victim buffer (Column 1 lines 10-12 and further in Column 15 lines 25-51 of Van Doren).

Hovis and Van Doren are analogous art because they are from the same field of endeavor, namely memory systems.

At the time of invention it would have been obvious to one of ordinary skill in the art, having both the teachings of Hovis and Van Doren before him/her, to integrate the victim buffers of Van Doren into the system of Hovis so displaced data from the cache has temporary storage.

The motivation for doing so would be that, "each CPU may also include victim buffers for temporarily storing data which is displaced from its cache (Column 1 lines 10-12 of Van Doren)."

Therefore, it would have been obvious to combine Hovis with Van Doren to obtain the invention as specified in claims 14, 16-17, 22-23, and 25-29.

As per dependent claim **16**, the combination of Hovis and Van Doren teach, locating a pointer and subsequently finding a compressed memory location based at

least in part on the pointer if the tag match resulted in a miss for the memory operation for a read miss (Column 3 line 54 to Column 4 line 9 of Hovis).

As per dependent claim **17**, the combination of Hovis and Van Doren teach, compressing the data and storing it in a compressed memory location for the memory operation for a write miss (Column 4 lines 34-45 of Hovis).

As per independent claim **22**, Hovis teach,

- a processor; and a memory interface, coupled to the processor, with a: (Figure 4 items 10 and 22).
- a first cache to store a plurality of tags for a compression cache; of a main memory coupled to the memory interface, the compression cache to store a plurality of uncompressed data; (Figure 1 as taught in Column 2 lines 35-37)
- a memory controller to schedule an uncompressed data access from the compression cache if a tag match operation between the plurality of tags and an access request results in a hit; (Column 3 lines 54-57)
- an offset calculator to provide an offset relative to the start for a Compressed Memory Pointer Table (CMPT) of the main memory that is to store pointers to compressed data stored in a compressed memory of the main memory, based on an actual address of a data being compressed; and (Column 3 lines 23-40 taught as the n+1 address)
- and a second cache to store a plurality of most recently used pointers for the CMPT (Column 3 lines 28-40).

Van Doren teach,

- a victim buffer to store at least one the entry that has been evicted from the compression cache; (Column 1 lines 10-12).

As per dependent claim **23**, the combination of Hovis and Van Doren teach, wherein the memory interface is incorporated within a processor or a chipset (Figure 4 of Hovis). *The Examiner notes that item 10 of Figure 4 is shown as a part of the whole system. Accordingly, item 10 is part of a chipset.*

As per dependent claim **25**, the combination of Hovis and Van Doren teach, wherein the entry is evicted based on a first in first out (FIFO) protocol (Column 4 lines 33-38 of Hovis).

As per independent claim **26**, Hovis teach,

- a processor, coupled to a memory bridge, the memory bridge to comprise; (Figure 4 also as taught in Column 3 lines 40-52)
- a first cache to store a plurality of tags for a compression cache of a main memory coupled to the memory bridge, the first cache to perform a tag match operation between the plurality of tags and an incoming memory address; (Figure 1 as taught in Column 2 lines 35-37)
- a memory controller to schedule an uncompressed data access from the compression cache if a tag match operation between the plurality of tags and an access request results in a hit; (Column 3 lines 54-57)
- an offset calculator to provide an offset relative to the start for a Compressed Memory Pointer Table (CMPT) of the main memory that is to

store pointers to compressed data stored in a compressed memory of the main memory, based on an actual address of a data being compressed; and (Column 3 lines 23-40 taught as the n+1 address)

- a second cache to store a plurality of pointers for the CMPT and (Column 3 lines 28-40).
- a main memory, coupled to the memory bridge, to comprise a (Figure 4 item 10 of Hovis)
- compression cache to store a plurality of uncompressed data; (Figure 1 as taught in Column 2 lines 35-37)
- a compressed memory to store a plurality of compressed data; (Figure 1 as taught in Column 2 lines 37-38)
- and a compressed memory pointer table (CMPT) to store a plurality of pointers (Column 1 lines 44-51)

Van Doren teach,

- a victim buffer to store at least one the entry that has been evicted from the compression cache; (Column 1 lines 10-12).

As per dependent claim **27**, the combination of Hovis and Van Doren teach, wherein the compression cache is a sectored cache (the sectored cache being taught by Hovis as segments of memory within the uncompressed storage cache in Column 2 lines 50-51).

As per dependent claim **28**, the combination of Hovis and Van Doren teach, wherein the compression cache has a plurality of associated tags that are incorporated within the memory bridge (Column 3 lines 3-15 of Hovis).

As per dependent claim **29**, the combination of Hovis, Harris, and Van Doren teach, wherein the plurality of pointers are to the plurality of compressed data based on a plurality of cache block addresses (Column 3 lines 3-8 of Hovis).

Claims **5-8** and **10-13**, are rejected under 35 U.S.C. 103(a) as being obvious over Hovis in view of Harris and further in view of Van Doren.

As per dependent claim **5**, the combination of Hovis and Harris teach, a CMPT offset calculator to provide an offset relative to the start of the CMPT based on an actual address of the data being compressed (Column 3 lines 23-40 of Hovis taught as the n+1 address).

The combination of Hovis and Harris does not teach, a victim buffer to store at least one the entry that has been evicted from the compression cache.

Van Doren teach, a victim buffer to store at least one the entry that has been evicted from the compression cache (Column 1 lines 10-12).

Hovis and Harris and Van Doren are analogous art because they are from the same field of endeavor, namely memory systems.

At the time of invention it would have been obvious to one of ordinary skill in the art, having both the teachings of Hovis and Harris, and Van Doren before him/her, to integrate the victim buffers of Van Doren into the system of Hovis and Harris so displaced data from the cache has temporary storage.

The motivation for doing so would be that, "each CPU may also include victim buffers for temporarily storing data which is displaced from its cache (Column 1 lines 10-12 of Van Doren)."

Therefore, it would have been obvious to combine Hovis and Harris with Van Doren to obtain the invention as specified in claims 5-8 and 10-13.

As per dependent claim **6**, the combination of Hovis, Harris, and Van Doren teach, wherein the memory interface is incorporated within a processor or a chipset (Figure 4 of Hovis). *The Examiner notes that item 10 of Figure 4 is shown as a part of the whole system. Accordingly, item 4 is part of a chipset.*

As per dependent claim **7**, the combination of Hovis, Harris, and Van Doren teach, wherein the apparatus is incorporated within a memory controller hub (MCH) of the chipset (Figure 4 item 24 of Hovis).

As per dependent claim **8**, the combination of Hovis, Harris, and Van Doren, teach, wherein the entry is to be evicted based on a first in first out (FIFO) protocol (Column 4 lines 33-38 of Hovis).

As per independent claim **10**, Hovis teach,

- a first cache to store a plurality of tags for a compression cache of a main memory coupled to the memory interface, the compression cache to store a plurality of uncompressed data; (Figure 1 as taught in Column 2 lines 35-37)
- an offset calculator to provide an offset relative to the start for a Compressed Memory Pointer Table (CMPT) of the main memory that is to

store pointers to compressed data stored in a compressed memory of the main memory, based on an actual address of a data being compressed; and (Column 3 lines 23-40 taught as the n+1 address).

- a second cache to store a plurality of pointers for the CMPT (Column 3 lines 28-40).

Van Doren teach,

- a victim buffer to store at least one the entry that has been evicted from the compression cache and to directly supply the at least one entry to a requester if a tag match occurs in the victim buffer (Column 1 lines 10-12 and further in Column 15 lines 25-51).

Harris teach,

- the apparatus to assign a higher priority to compressed memory read operations in comparison to other operations (Figure 4 as taught in Column 7 line 58 to Column 8 line 24 of Harris).

As per dependent claim **11**, the combination of Hovis, Harris, and Van Doren teach, wherein the memory interface is incorporated within a processor or a chipset (Figure 4 of Hovis). *The Examiner notes that item 10 of Figure 4 is shown as a part of the whole system. Accordingly, item 10 is part of a chipset.*

As per dependent claim **12**, the combination of Hovis, Harris, and Van Doren teach, wherein the apparatus is incorporated within a memory controller hub (MCH) of the chipset (Figure 4 item 24 of Hovis).

As per dependent claim **13**, the combination of Hovis, Harris, and Van Doren teach, wherein the entry is evicted based on a first in first out (FIFO) protocol (Column 4 lines 33-38 of Hovis).

Response to Arguments

Applicant's arguments filed 29 October 2007 have been carefully and fully considered but are moot in view of the new ground(s) of rejection as necessitated by amendment.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew Bradley whose telephone number is (571) 272-8575. The examiner can normally be reached on 6:30-3:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald A. Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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